Dual, High Voltage, Isolated MOSFET Driver

Features

- ±400V input to output isolation
- ±700V isolation between outputs
- No external voltage supply required
- Dual isolated output drivers
- Option of internal or external clock

Applications

- Telecommunications
- Modems
- Solid state relays
- High side switches
- High end audio switches
- Avionics
- ATE

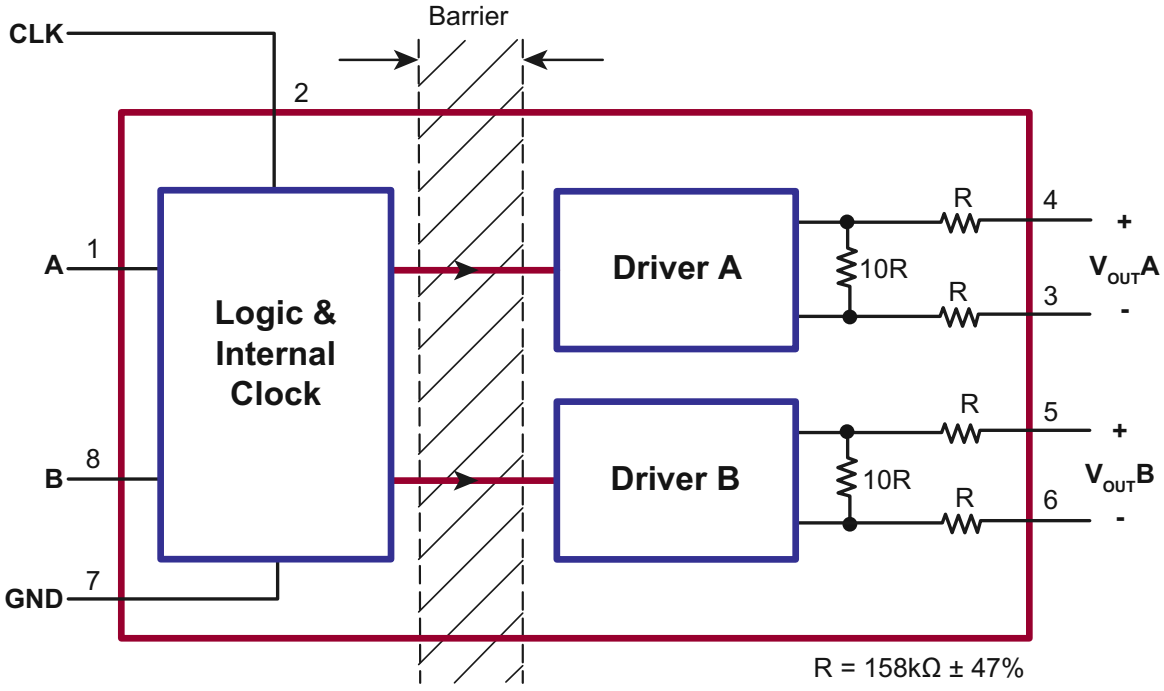
General Description

The Supertex HT0440 is a dual, high voltage, isolated MOSFET driver utilizing Supertex's proprietary HVCMOS® technology. It is designed to drive discrete MOSFETs configured as bidirectional or unidirectional switches. It can drive N-channel MOSFETs as high-side switches up to 400V. The HT0440 generates two independent DC isolated voltages to the outputs, $V_{OUT}A$ and $V_{OUT}B$ when logic inputs A and B are at logic high.

The internal clock of the HT0440 can be disabled by applying an external clock signal to the CLK pin. This allows the power dissipation and AC characteristics to be tailored to meet specific needs. The CLK pin should be connected to ground when not in use. The HT0440 does not require any external power supplies, the internal supply voltage is supplied by either of the two logic inputs, A or B, when they are at logic high.

For detailed circuit application information, please refer to application note AN-D26.

Block Diagram



Ordering Information

Part Number	Package Options	Packing
HT0440K6-G	10-Lead (3x4) DFN	3000/Reel
HT0440LG-G	8-Lead SOIC (Narrow Body)	2500/Reel

-G denotes a lead (Pb)-free / RoHS compliant package

Absolute Maximum Ratings

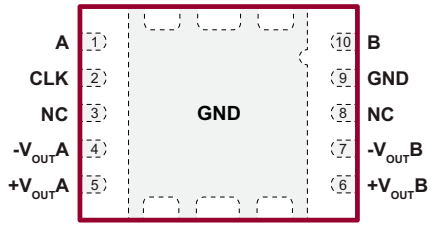
Parameter	Value
Input to output isolation voltage, V_{ISO}	±400V
Logic input voltage, V_A, V_B	-0.5 to +7.0V
Maximum junction temperature	+125°C
Storage temperature	-55°C to +150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

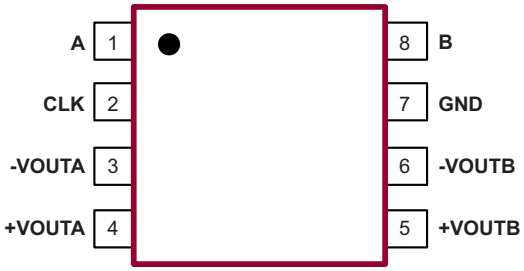
Typical Thermal Resistance

Package	θ_{ja}
10-Lead DFN	40°C/W
8-Lead SOIC (Narrow Body)	101°C/W

Pin Configurations



10-Lead DFN
(top view)



8-Lead SOIC (Narrow Body)
(top view)

Product Marking



Y = Last Digit of Year Sealed
W = Code for Week Sealed
L = Lot Number
___ = "Green" Packaging

Package may or may not include the following marks: Si or

10-Lead DFN



YY = Year Sealed
WW = Week Sealed
L = Lot Number
_____ = "Green" Packaging

Package may or may not include the following marks: Si or

8-Lead SOIC (Narrow Body

Recommended Operating Conditions

Sym	Parameter	Min	Typ	Max	Units	Conditions
CLK	External clock frequency	0.5	-	2.0	MHz	---
V_{IHCLK}	Clock input high voltage	3.15	-	5.5	V	---
V_{ILCLK}	Clock input low voltage	0	-	0.5	V	---
V_{IH}	Logic input high voltage	3.15	-	5.5	V	---
V_{IL}	Logic input low voltage	0	-	0.5	V	---
T_A	Operating temperature	-40	-	+85	°C	---

DC Electrical Characteristics *(T_A = 25°C unless otherwise specified)*

Sym	Parameter	Min	Typ	Max	Units	Conditions
$I_{HA} + I_{HB}$	Total logic high input current	-	-	300	µA	V_A = 3.5V, V_B = 3.5V, CLK = 0V
		-	-	500	µA	V_A = 3.5V, V_B = 3.5V, CLK = 500kHz
		-	-	2.0	mA	V_A = 3.5V, V_B = 3.5V, CLK = 2.0MHz
		-	-	1.0	mA	V_A = 5.5V, V_B = 5.5V, CLK = 0V
		-	-	2.0	mA	V_A = 5.5V, V_B = 5.5V, CLK = 500kHz
V_{OUTA}, V_{OUTB}	Output voltage	6.0	-	-	V	V_A = 3.15V, V_B = 3.15V, CLK = 0V, no load
		5.0	-	-	V	V_A = 3.15V, V_B = 3.15V, CLK = 500kHz, no load
		6.0	-	-	V	V_A = 3.15V, V_B = 3.15V, CLK = 2.0MHz, no load
		10.0	-	-	V	V_A = 4.5V, V_B = 4.5V, CLK = 0V, no load
		8.0	-	-	V	V_A = 4.5V, V_B = 4.5V, CLK = 500KHz, no load
I_{ILA}	Logic low input A current	-	-	10	µA	V_A = 0.5V, V_B = high
I_{ILB}	Logic low input B current	-	-	10	µA	V_A = high, V_B = 0.5V
I_{ILQ}	Quiescent current	-	-	10	µA	V_A = 0.5V, V_B = 0.5V
V_{ISO}	Input to output isolation voltage	±400	-	-	V	---
V_{CISO}	Output to output isolation voltage	±700	-	-	V	---

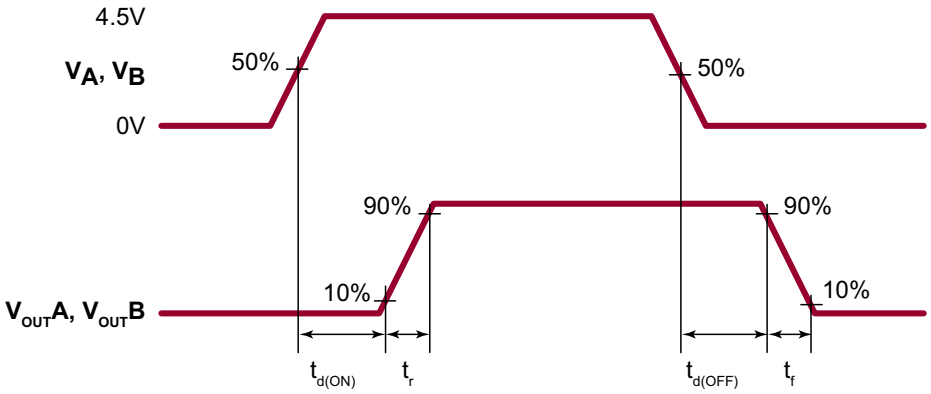
AC Electrical Characteristics *(T_A =25°C unless otherwise specified)*

Sym	Parameter	Min	Typ	Max	Units	Conditions
$t_{d(ON)}$	Turn-ON delay time	-	-	50	µs	See timing diagram and test circuit CLK = 0V, CL = 600pF
t_r	Rise time	-	-	650	µs	
$t_{d(OFF)}$	Turn-OFF delay time	-	-	150	µs	
t_f	Fall time	-	-	3.0	ms	

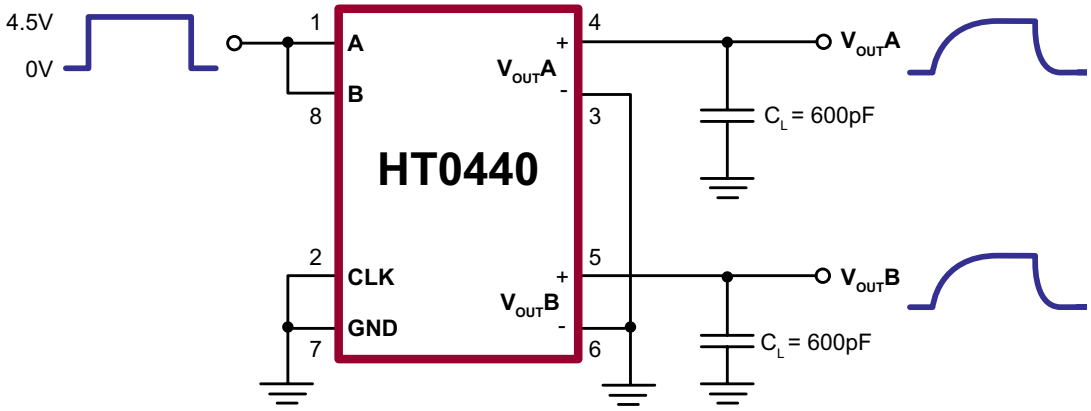
Truth Table

A	B	CLK	V_{OUT}A	V_{OUT}B	Internal Clock
0	0	0	OFF	OFF	OFF
0	⌐	0	OFF	ON	ON
⌐	0	0	ON	OFF	ON
1	1	0	ON	ON	ON
0	0	CLK	OFF	OFF	OFF
0	⌐	CLK	OFF	ON	OFF
⌐	0	CLK	ON	OFF	OFF
1	1	CLK	ON	ON	OFF

Timing Diagram

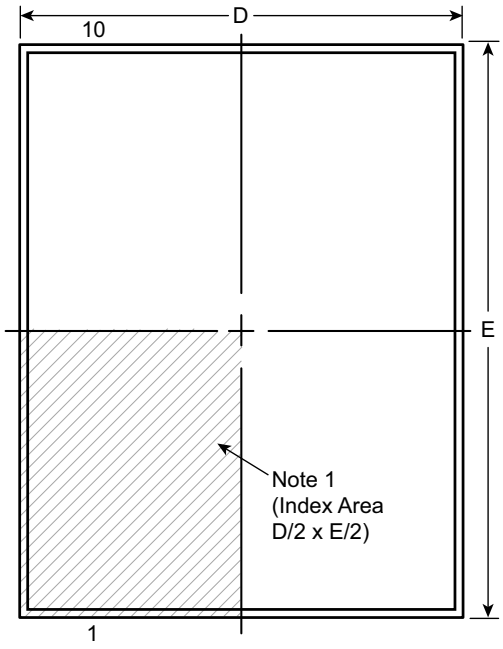


Test Circuit

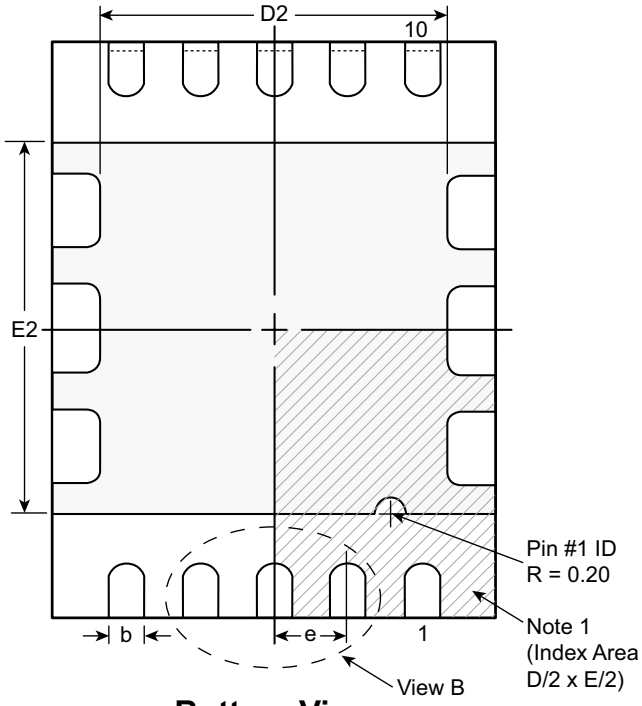


10-Lead DFN Package Outline (K6)

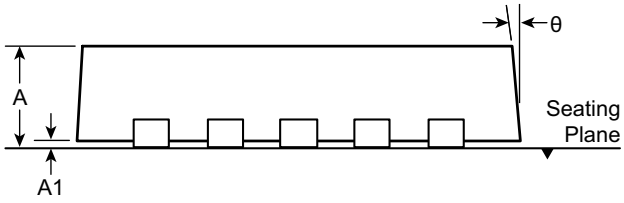
3.00x4.00mm body, 1.00mm height (max), 0.50mm pitch



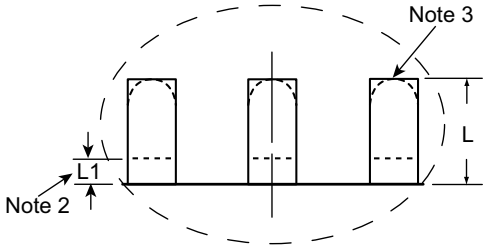
Top View



Bottom View



Side View



View B

Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.*
3. *The inner tip of the lead may be either rounded or square.*

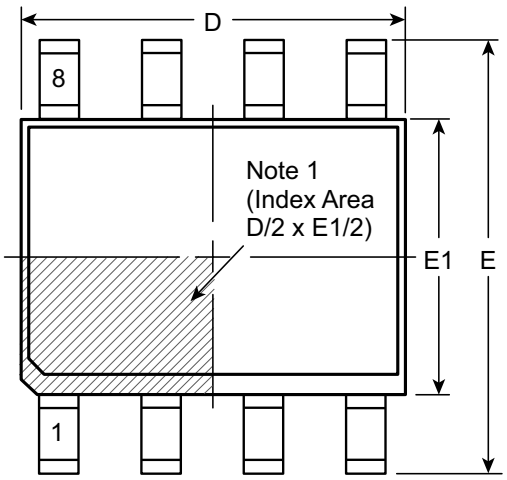
Symbol		A	A1	b	D	D2	E	E2	e	L	L1	θ
Dimension (mm)	MIN	0.80	0.00	0.18	2.95	2.20	3.95	2.50	0.50 BSC	0.30	0.00	0°
	NOM	0.90	0.02	0.25	3.00	2.35	4.00	2.65		0.40	-	-
	MAX	1.00	0.05	0.30	3.05	2.45	4.05	2.75		0.50	0.15	14°

Drawings not to scale.

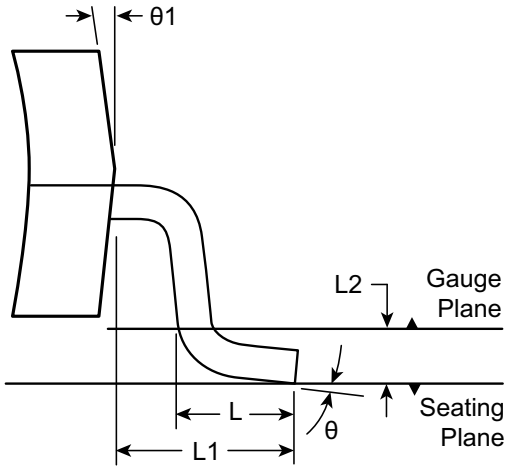
Supertex Doc. #: *DSPD-10DFNK63X4P050, Version A072611*

8-Lead SOIC (Narrow Body) Package Outline (LG)

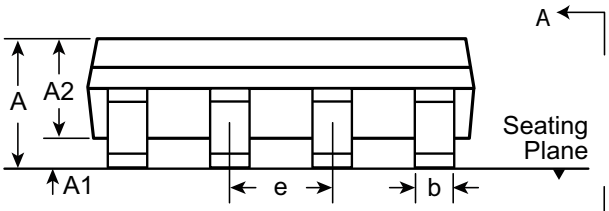
4.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



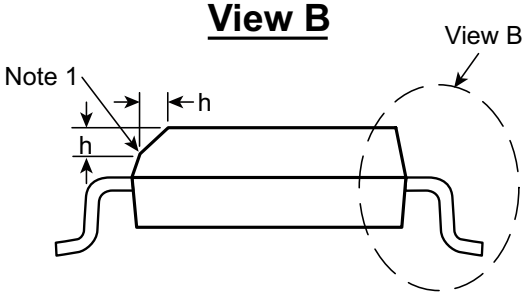
Top View



View B



Side View



View A-A

Note:

1. *This chamfer feature is optional. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.35*	0.10	1.25	0.31	4.80*	5.80*	3.80*	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	4.90	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.65*	0.51	5.00*	6.20*	4.00*		0.50	1.27			8°	15°

JEDEC Registration MS-012, Variation AA, Issue E, Sept. 2005.
** This dimension is not specified in the JEDEC drawing.*
Drawings are not to scale.
***Supertex Doc. #:** DSPD-8SOLGTG, Version I041309.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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